# AU5422G: 1.8 V TO 3.3 V HIGH PERFORMANCE LVCMOS CLOCK BUFFER OUTPUT, ULTRA LOW JITTER BUFFER

## General Description

The AU5422G is a high-performance LVCMOS clock buffer family of devices. It has an additive phase jitter of 50 fs RMS.

The AU5422G supports a synchronous glitch-free output enable (OE) function to eliminate any potential intermediate incorrect output clock cycles when enabling or disabling outputs. It can operate from a 1.8 V to 3.3 V supply.

**Typical Applications:**

- 5G, 4G Basestations
- Telecom Equipment
- Servers

## Features

- High-performance 1:2
- LVCMOS clock buffer
- Very low pin-to-pin skew: <50 ps
- Very low additive jitter: <50 fs
- Supply voltage: 1.8 V to 3.3 V
- 3.3 V tolerant input clock
- $F_{MAX}$ = 200 MHz
- Integrated serial termination for 50 Ω channel
- Packaged in 8pin, 2 × 2 mm DFN packages

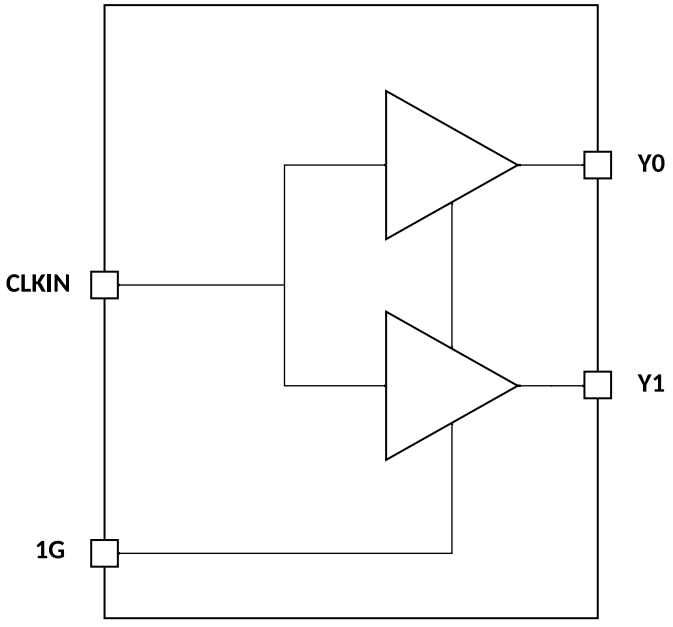


**Figure 1 Functional Overview of AU5422G**

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# 1 Pin Description

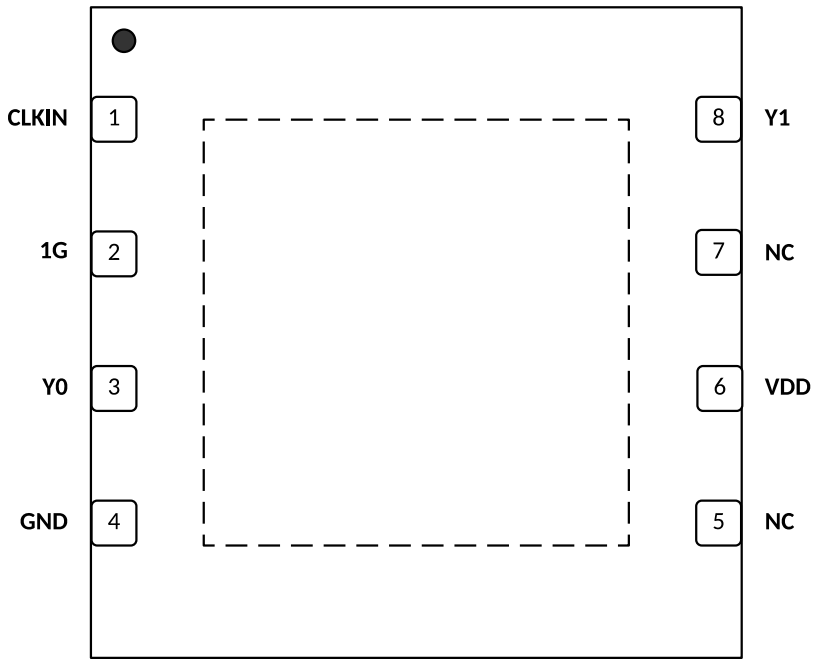


**Figure 2 AU5422G Pin Configuration**

**Table 1 Detailed Pin Description**

| Pin Name | Pin Number | Functionality and Description |
|---|---|---|
| Y0 | 3 | LVCMOS output 0 |
| Y1 | 8 | LVCMOS output 1 |
| NC | 5 | Not Connected |
| NC | 7 | Not Connected |
| CLKIN | 1 | Single Ended Input Clock |
| 1G | 2 | All outputs enable/disable |
| VDD | 6 | Core Supply Voltage, VDD |
| GND | 4 | Ground |

## 2 Electrical Specifications

**Table 2 Absolute Maximum Ratings**

| Parameters | Conditions | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Supply Voltage, $V_{DD}$ | | | 3.6 | | 3.6 | V |
| Output Enable and All Outputs | | | -0.4 | | $V_{DD}$+0.3 | V |
| Input voltage, CLKIN | | | -0.4 | | 3.465 | V |
| Ambient Operating Temperature, | | | -40 | | +105 | °C |
| Storage Temperature | | | -65 | | +150 | °C |
| Junction Temperature | | | | | +150 | °C |
| Soldering Temperature | | | | | +260 | °C |

Notes:

- Exceeding maximum ratings may shorten the useful life of the device.
- Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or at any other conditions beyond those indicated under the DC Electrical Characteristics is not implied. Exposure to Absolute-Maximum-Rated conditions for extended periods may affect device reliability or cause permanent device damage.

**Table 3 Recommended Operating Supply and Temperature**

| Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Ambient Operating Temperature | | -40 | | +105 | °C |
| Power Supply Voltage (Measured in respect to GND) | | +1.71 | | +3.465 | V |

**Table 4 DC Electrical Characteristics - $V_{DD}$ = 1.8 V ±5%**

| Parameter | Conditions | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Operating Voltage | | $V_{DD}$ | 1.71 | 1.8 | 1.89 | V |
| Input High Voltage, CLKIN[1] | | $V_{IH}$ | 0.7×$V_{DD}$ | | | V |
| Input Low Voltage, CLKIN[1] | | $V_{IL}$ | | | 0.3×$V_{DD}$ | V |
| Input High Voltage, 1G | | $V_{IH}$ | 1.6 | | $V_{DD}$ | V |
| Input Low Voltage, 1G | | $V_{IL}$ | | | 0.6 | V |
| Output High Voltage | $I_{OH}$ = -5 mA. | $V_{OH}$ | 1.4 | | | V |
| Output Low Voltage | $I_{OL}$ = 5 mA. | $V_{OL}$ | | | 0.2 | V |
| Nominal Output Impedance | | $Z_O$ | | 50 | | Ω |
| Input Capacitance | CLKIN, 1G pin. | $C_{IN}$ | | 5 | | pF |
| Operating Supply Current[2] | 0.001 MHz, $C_L$ = 5 pF. | $I_{DD}$ | | 0.7 | 1.7 | mA |
| | 0.008 MHz, $C_L$ = 5 pF. | | | 0.7 | 1.7 | |
| | 40 MHz, $C_L$ = 5 pF. | | | 7 | 8.3 | |
| | 100 MHz, $C_L$ = 5 pF. | | | 15.4 | 18.5 | |
| | 156.25 MHz, $C_L$ = 5 pF. | | | 23.2 | 29.5 | |
| | 200 MHz, $C_L$ = 5 pF. | | | 25.2 | 36.8 | |

Notes:

1. Nominal switching threshold is VDD/2.
2. TA = -40 °C to +105 °C unless stated otherwise.

**Table 5 DC Electrical Characteristics - $V_{DD}$ = 2.5 V ±5%**

| Parameter | Conditions | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Operating Voltage | | $V_{DD}$ | 2.375 | 2.5 | 2.625 | V |
| Input High Voltage, CLKIN[1] | | $V_{IH}$ | 0.7×$V_{DD}$ | | | V |
| Input Low Voltage, CLKIN[1] | | $V_{IL}$ | | | 0.3×$V_{DD}$ | V |
| Input High Voltage, 1G | | $V_{IH}$ | 1.8 | | $V_{DD}$ | V |
| Input Low Voltage, 1G | | $V_{IL}$ | | | 0.7 | V |
| Output High Voltage | $I_{OH}$ = -8 mA. | $V_{OH}$ | 1.9 | | | V |
| Output Low Voltage | $I_{OL}$ = 8 mA. | $V_{OL}$ | | | 0.5 | V |
| Nominal Output Impedance | | $Z_O$ | | 50 | | Ω |
| Input Capacitance | CLKIN, 1G pin. | $C_{IN}$ | | 5 | | pF |
| Operating Supply Current[2] | 0.001 MHz, $C_L$ = 5 pF. | $I_{DD}$ | | 0.9 | 2 | mA |
| | 0.008 MHz, $C_L$ = 5 pF. | | | 0.9 | 2 | |
| | 40 MHz, $C_L$ = 5 pF. | | | 9.7 | 11.2 | |
| | 100 MHz, $C_L$ = 5 pF. | | | 22 | 26.5 | |
| | 156.25 MHz, $C_L$ = 5 pF. | | | 33.2 | 42.7 | |
| | 200 MHz, $C_L$ = 5 pF. | | | 36.7 | 52.4 | |

Notes:

1. Nominal switching threshold is VDD/2.
2. TA = -40 °C to +105 °C unless stated otherwise.

**Table 6 DC Electrical Characteristics - $V_{DD}$ = 3.3 V ±5%**

| Parameter | Conditions | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Operating Voltage | | $V_{DD}$ | 3.135 | 3.3 | 3.465 | V |
| Input High Voltage, CLKIN[1] | | $V_{IH}$ | 0.7×$V_{DD}$ | | | V |
| Input Low Voltage, CLKIN[1] | | $V_{IL}$ | | | 0.3×$V_{DD}$ | V |
| Input High Voltage, 1G | | $V_{IH}$ | 2.1 | | $V_{DD}$ | V |
| Input Low Voltage, 1G | | $V_{IL}$ | | | 0.8 | V |
| Output High Voltage | $I_{OH}$ = -12 mA. | $V_{OH}$ | 2.4 | | | V |
| Output Low Voltage | $I_{OL}$ = 12 mA. | $V_{OL}$ | | | 0.7 | V |
| Nominal Output Impedance | | $Z_O$ | | 50 | | Ω |
| Input Capacitance | CLKIN, 1G pin. | $C_{IN}$ | | 5 | | pF |
| Operating Supply Current[2] | 0.001 MHz, $C_L$ = 5 pF. | $I_{DD}$ | | 1.2 | 2.2 | mA |
| | 0.008 MHz, $C_L$ = 5 pF. | | | 1.2 | 2.2 | |
| | 40 MHz, $C_L$ = 5 pF. | | | 12.6 | 15.5 | |
| Operating Supply Current[2] | 100 MHz, $C_L$ = 5pF. | $I_{DD}$ | | 29.4 | 35.3 | |
| | 156.25 MHz, $C_L$ = 5pF. | | | 44.1 | 57.2 | |
| | 200 MHz, $C_L$ = 5pF. | | | 50.9 | 72.7 | |

Notes:

1. Nominal switching threshold is VDD/2.
2. TA = -40 °C to +105 °C unless stated otherwise.

**Table 7 AC Electrical Characteristics - $V_{DD}$ = 1.8 V ±5%**

| Parameter | Conditions | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Input Frequency | DC coupled | | 0 | | 200 | MHz |
| | AC coupled | | 0.1 | | 200 | MHz |
| Input swing, AC coupled mode | CLKIN biased at 0.5VDD | $V_{SWING\_AC}$ | 0.5 | | | V |
| Output Rise Time (5 pF load)[2] | 0.36 V to 1.44 V, $C_L$ = 5 pF. | $t_{OR}$ | | 0.65 | 1.2 | ns |
| Output Fall Time (5 pF load)[2] | 1.44 V to 0.36 V, $C_L$ = 5 pF. | $t_{OF}$ | | 0.65 | 1.2 | ns |
| Start-up Time | Part start-up time for valid outputs after VDD ramp-up. | $t_{START-UP}$ | | | 3 | ms |
| Propagation Delay[3] | | $t_{PD}$ | 0.24 | | 1.6 | ns |
| Buffer Additive Phase Jitter, RMS | 156.25 MHz, Integration Range: 12 kHz – 20 MHz. | $t_{JIT}$ | | | 0.06 | ps |
| Output to Output Skew | Rising edges at VDD/2.[1] | $t_{SK}$ | | 35 | 50 | ps |
| Device to Device Skew | Rising edges at VDD/2. | | | | 200 | ps |
| Output Enable Time | $C_L$ ≤ 5 pF Frequency = 25 Mhz | $t_{EN}$ | | | 3 | cycles |
| | $C_L$ ≤ 5 pF Frequency = 200 Mhz | $t_{EN}$ | | | 5 | cycles |
| Output Disable Time | $C_L$ ≤ 5 pF. Frequency = 25 Mhz | $t_{DIS}$ | | | 3 | cycles |
| | $C_L$ ≤ 5 pF Frequency = 200 Mhz | $t_{DIS}$ | | | 5 | cycles |
| Duty Cycle | DC couple mode | $t_{DC}$ | | 50 | | % |
| | AC couple mode(AC swing > 0.8V) | | | | | |

Notes:

1. Between any 2 outputs with equal loading.
2. TA = -40 °C to +105 °C unless stated otherwise.
3. With rail to rail input clock

**Table 8 AC Electrical Characteristics - $V_{DD}$ = 2.5 V ±5%**

| Parameter | Conditions | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Input Frequency | DC coupled | | 0 | | 200 | MHz |
| | AC coupled | | 0.1 | | 200 | MHz |
| Input swing, AC coupled mode | CLKIN biased at 0.5VDD | $V_{SWING\_AC}$ | 0.5 | | | V |
| Output Rise Time (5 pF load)[2] | 0.5 V to 2.0 V, $C_L$ = 5 pF. | $t_{OR}$ | | 0.63 | 1.2 | ns |
| Output Fall Time (5 pF load)[2] | 2.0 V to 0.5 V, $C_L$ = 5 pF. | $t_{OF}$ | | 0.63 | 1.2 | ns |
| Start-up Time | Part start-up time for valid outputs after $V_{DD}$ ramp-up. | $t_{START-UP}$ | | | 3 | ms |

| Parameter | Conditions | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Propagation Delay[3] | | $t_{PD}$ | 0.24 | | 1.6 | ns |
| Buffer Additive Phase Jitter, RMS | 156.25 MHz, Integration Range: 12 kHz – 20 MHz. | $t_{JIT}$ | | | 0.06 | ps |
| Output to Output Skew | Rising edges at $V_{DD}/2$[1] | $t_{SK}$ | | 35 | 50 | ps |
| Device to Device Skew | Rising edges at $V_{DD}/2$ | $t_{SKD}$ | | | 200 | ps |
| Output Enable Time | $C_L \le 5$ pF Frequency = 25Mhz | $t_{EN}$ | | | 3 | cycles |
| | $C_L \le 5$ pF Frequency = 200Mhz | $t_{EN}$ | | | 5 | cycles |
| Output Disable Time | $C_L \le 5$ pF. Frequency = 25Mhz | $t_{DIS}$ | | | 3 | cycles |
| | $C_L \le 5$ pF Frequency = 200Mhz | $t_{DIS}$ | | | 5 | cycles |
| Duty Cycle | DC couple mode | $t_{DS}$ | | 50 | | % |
| | AC couple mode(AC swing > 0.8V) | | | | | |

Notes:

1. Between any 2 outputs with equal loading.
2. TA = -40 °C to +105 °C unless stated otherwise.
3. With rail to rail input clock

**Table 9 AC Electrical Characteristics - $V_{DD}$ = 3.3 V ±5%**

| Parameter | Conditions | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Input Frequency | DC coupled | | 0 | | 200 | MHz |
| | AC coupled | | 0.1 | | 200 | MHz |
| Input swing, AC coupled mode | CLKIN biased at 0.5VDD | $V_{SWING\_AC}$ | 0.5 | | | V |
| Output Rise Time (5 pF load)[2] | 0.66 V to 2.64 V, CL = 5 pF. | $t_{OR}$ | | 0.61 | 1.2 | ns |
| Output Fall Time (5 pF load)[2] | 2.64 V to 0.66 V, CL = 5 pF. | $t_{OF}$ | | 0.61 | 1.2 | ns |
| Start-up Time | Part start-up time for valid outputs after VDD ramp-up. | $t_{START-UP}$ | | | 3 | ms |
| Propagation Delay[3] | | $t_{PD}$ | 0.24 | | 1.6 | ns |
| Buffer Additive Phase Jitter, RMS | 156.25 MHz, Integration Range: 12 kHz – 20 MHz. | $t_{JIT}$ | | | 0.05 | ps |
| Output to Output Skew | Rising edges at VDD/2[1] | $t_{SK}$ | | 35 | 50 | ps |
| Device to Device Skew | Rising edges at VDD/2. | $t_{SKD}$ | | | 200 | ps |
| Output Enable Time | $C_L \le 5$ pF Frequency = 25Mhz | $t_{EN}$ | | | 3 | cycles |
| | $C_L \le 5$ pF Frequency = 200Mhz | $t_{EN}$ | | | 5 | cycles |
| Output Disable Time | $C_L \le 5$ pF. Frequency = 25Mhz | $t_{DIS}$ | | | 3 | cycles |
| | $C_L \le 5$ pF Frequency = 200Mhz | $t_{DIS}$ | | | 5 | cycles |

| Parameter | Conditions | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Duty Cycle | DC couple mode | $t_{DC}$ | | 50 | | % |
| | AC couple mode(AC swing > 0.8V) | | | | | |

Notes:

1. Between any 2 outputs with equal loading.
2. TA = -40 °C to +105 °C unless stated otherwise.
3. With rail to rail input clock

**Table 10 ESD Ratings**

| Parameter | Conditions | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| ESD (Human Body Model) | AEC-Q100-002 | $ESD_{HBM}$ | - | 2000 | - | V |
| ESD(Charged Device Model) | AEC-Q100-011 | $ESD_{CDM}$ | - | 500 | - | V |

**Table 11 Thermal Characteristics**

| Package | ΘJA | Units |
|---|---|---|
| 8-DFN | 75 | °C/W; still air |

# 3 Functional Description

## 3.1Output Logic Tables

**Table 12 Output Logic Tables**

| Inputs | | Output |
|---|---|---|
| CLKIN | 1G | Yn |
| X | L | L |
| L | H | L |
| H | H | H |

## 4 Typical Application Diagram

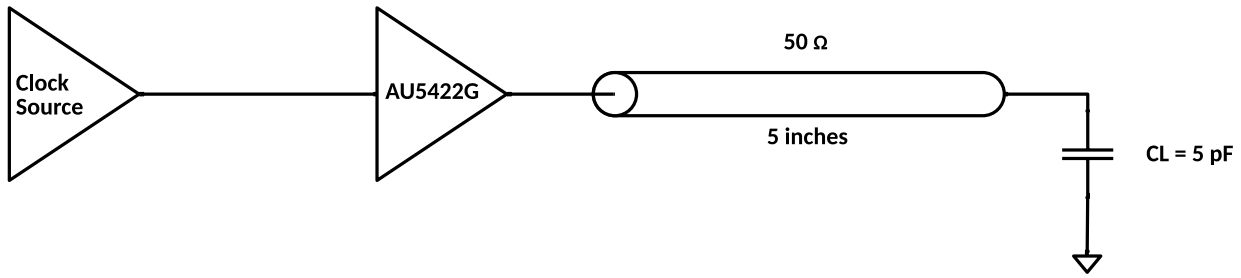


**Figure 3 AU5422G Typical Application Load – DC Coupled Mode**

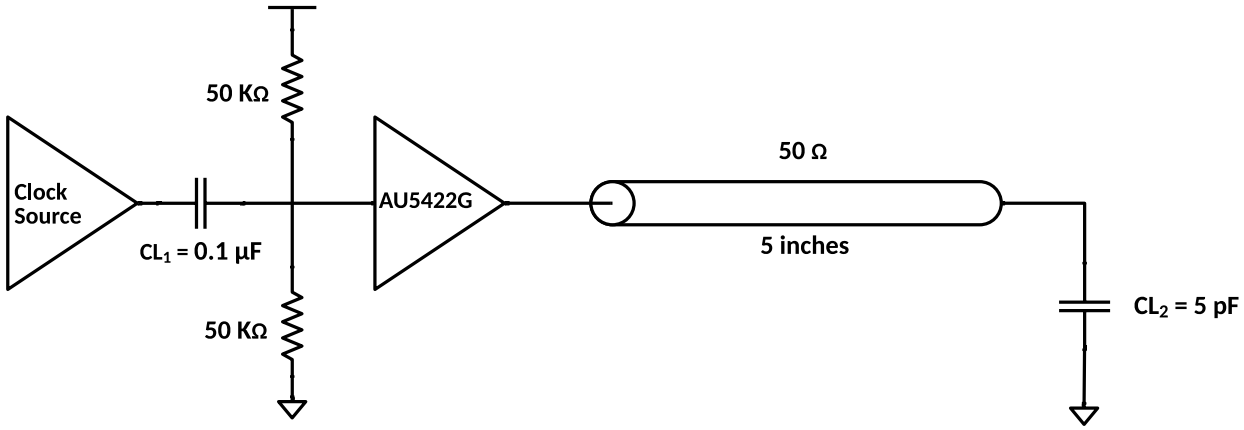


**Figure 4 AU5422G Typical Application Load - AC Coupled Mode**

## 5 Package Information

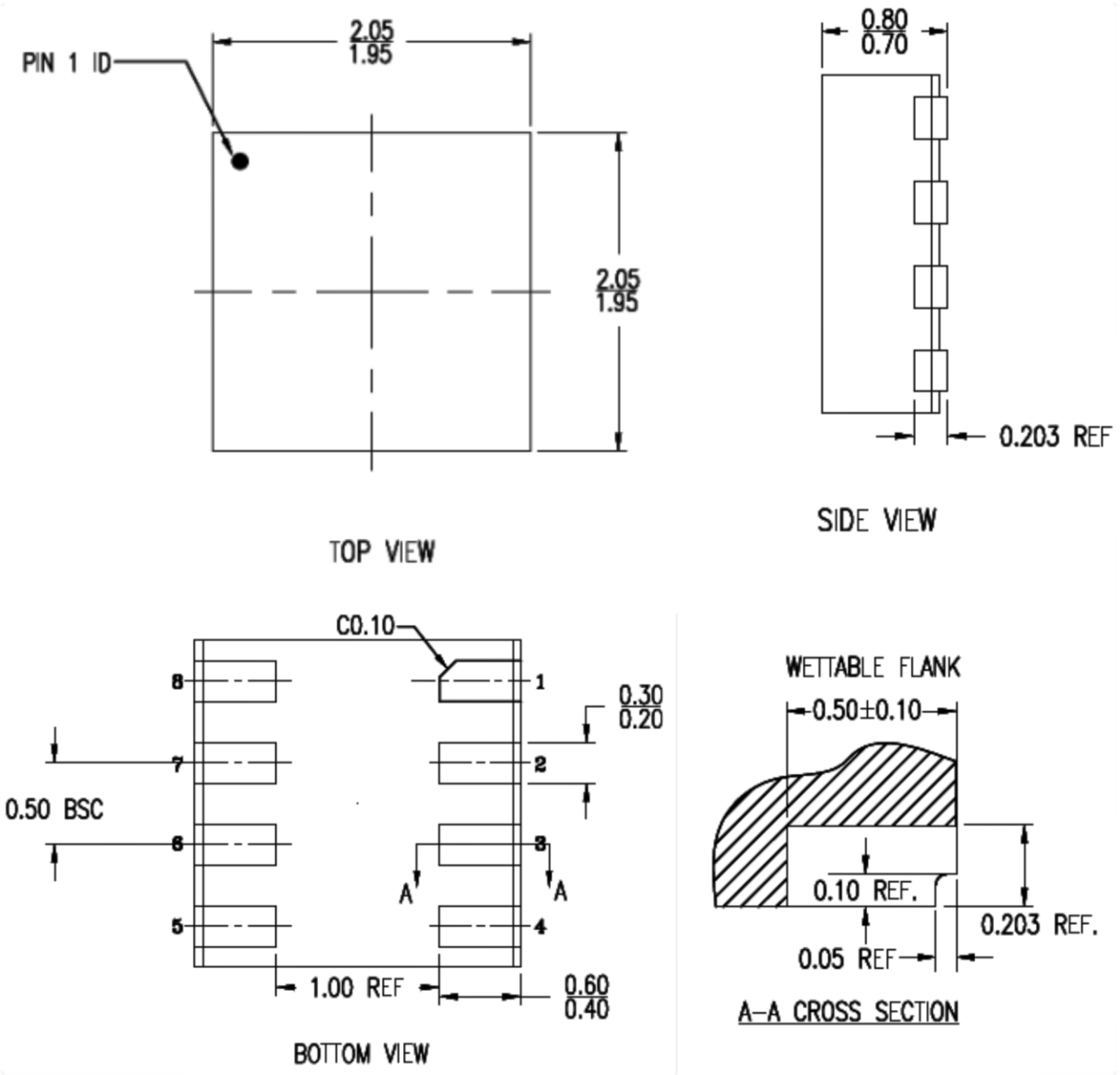


**Figure 5 AU5422G Cross Sections**

Note:

1. All dimensions and tolerences Conform to ANSI Y14.5M -1982
2. All dimensions are in millimeters (mm)

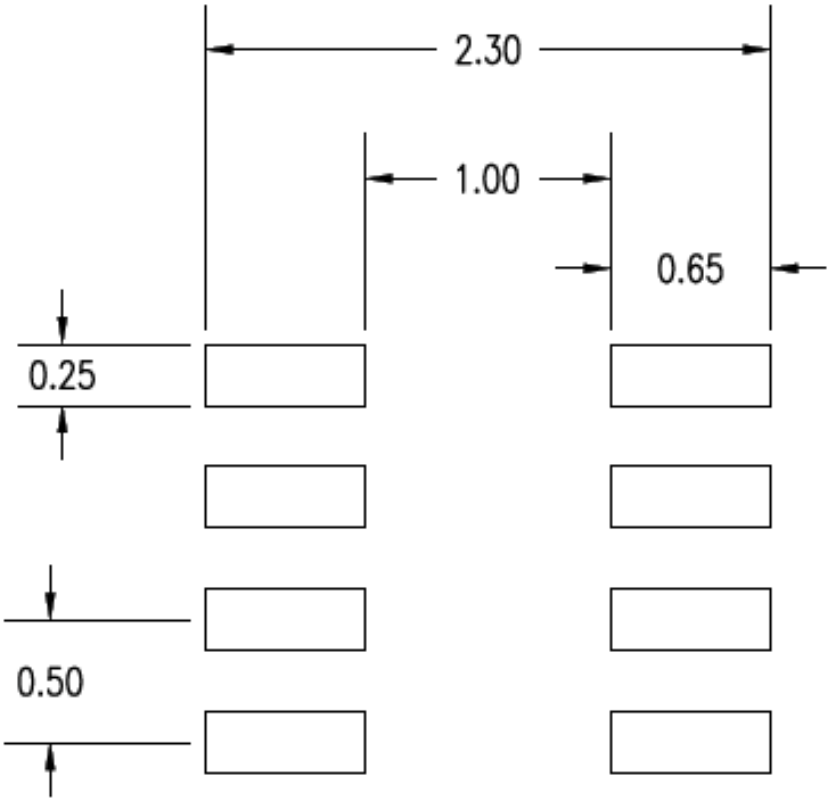


**Figure 6 Recommended Land Pattern Dimension**

Note:

1. All dimensions are in millimeters (mm)
2. All angles are in degrees
3. Land Pattern Recommendation per IPC-7351B Generic Requirement for Mount Design and Land Pattern

# 6 Ordering Information

**Table 13 Ordering Information for AU5422G**

| Ordering Part Number (OPN) | Marking | Package | Shipping Package | Temp. Range |
|---|---|---|---|---|
| AU5422BG-DNR[1] | 22BG | 8 Lead DFN<br>2 mm x 2 mm | Tape and Reel | –40 to 105°C |
| AU5422BG-DMR[1] | 22BG | 8 Lead DFN<br>2 mm x 2 mm | Tape and Reel | –40 to 85°C |
| AU5422BG-EVB | — | — | Evaluation Board | — |

Notes:

1. Add an R at the end of the OPN to denote tape and reel ordering option. Add a T at the end of the OPN to denote a tray option.

# 7 Revision History

**Table 14 Revision History**

| Version | Date | Description | Author |
|---|---|---|---|
| 0.1 | 7th March 2022 | AU5422G Data Sheet | Aurasemi |
| 0.2 | 30th March 2022 | Table 10 ESD Ratings added | Aurasemi |
| 0.3 | 25th May 2022 | Supply Current limits are updated | Aurasemi |
| 1.0 | 4th Aug 2022 | AU5422G Datasheet : Production Version released | Aurasemi |

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